IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket No.: **AZMT/002P1**	§	Serial No.: **10/730,758**
	§	
Filed: **December 8, 2003**	§	Group Art Unit: **2814**
	§	
In re Application of: **Nallan, et al.**	§	Confirmation No.: **3464**
	§	
	§	Examiner: **Ha, Nathan W.**

For: **METHOD AND APPARATUS FOR PACKAGING ELECTRONIC COMPONENTS**

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

REPLY BRIEF

In response to the Examiner's Answer dated August 16, 2006, please enter this Reply Brief. As this response is submitted within two months from the date of mailing of the Examiner's Answer, the Appellant believes that no fees are due in connection with this response. However, the Commissioner is hereby authorized to charge counsel's Deposit Account No. 50-3562 for any fees, including extension of time fees, required to make this response timely and acceptable to the Office.

REAL PARTY IN INTEREST

The real party in interest is Azimuth Industrial Co., Inc., located in Union City, California.

RELATED APPEALS AND INTERFERENCES

The Appellant knows of no related appeal and/or interference that may directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-14 are pending in the application. Claims 12-14 are withdrawn from consideration. Claims 1-11 stand rejected in view of several references as discussed below. The rejection of claims 1-11 based on the cited references is appealed. The pending claims are shown in the attached Appendix.

STATUS OF AMENDMENTS

No amendments to the claims were submitted in this application subsequent to final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention provides a method of packaging at least one component. In the embodiment of independent claim 1, a method of packaging at least one component includes providing a lid 104 having a plurality of vent holes 105. (¶ [0021]; Figs. 3, 7.) Sidewalls 302 are molded onto a substrate 202 to form a plurality of cavities 300 surrounding a component-mounting surface (ground plane 208). (¶[0020]; Figs. 2-3, 7.) A component 306 is mounted on the component-mounting surface 208 in each cavity 300. (¶ [0024]; Figs. 3, 7.) A curable adhesive 500 is applied to a top surface 310 of the sidewalls 302. (¶ [0025]; Figs. 5-7.) The lid 104 is placed upon the top surface 310 of the sidewalls 302 such that at least one vent hole 105 is aligned with each cavity 300. (¶ [0026]; Figs. 3, 7.) The adhesive 500 is then cured, wherein said vent hole 105 provides a path for outgassing during curing. (*Id.*) Said vent holes 104

are then sealed to form a component package assembly having a plurality of cavities 300, separated by sidewalls 302. (¶ [0027]; Figs. 5-7.) The component package assembly 116 is separated into a plurality of individual component packages 118. (¶ [0028]; Figs. 6-7.)

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-7 and 9-11 stand rejected under 35 USC §103(a) as being obvious in light of United States Patent No. 6,268,236, issued July 31, 2001 to *Miyawaki* (hereinafter *Miyawaki*) in view of United States Patent No. 4,897,508 issued January 30, 1990 to *Mahulikar, et al.*, (hereinafter *Mahulikar*).

2. Claim 8 stands rejected under 35 USC §103(a) as being obvious in light of *Miyawaki* in view of *Mahulikar*, as applied above, and further in view of United States Patent No. 5,776,799, issued July 7, 1998 to *Song, et al* (hereinafter *Song*).

ARGUMENT

Response to Examiner's Answer

In the Response to Argument section of the Examiner's Answer, the Examiner states that the main issue of Appellant's argument is "whether the cited references disclose a well known, or commonly used process such as molding." The Examiner further states, on page 6, lines 6-7, that "the Appellant insists that *Miyawaki* does not disclose the molding process as a conventional process." The Appellant strongly disagrees with the Examiner's overbroad characterization of the argument and further notes that the Examiner is mistaken with respect to the Appellant's argument regarding the teachings of *Miyawaki*.

Specifically, the Appellant asserts that the cited references fail to teach or suggest molding sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface in combination with the other limitations recited in claim 1, and not that the references fail to disclose that molding methods exist in the prior art at all.

As noted in the Appeal Brief, with reference to Figures 2A-2C, and in all other embodiments, *Miyawaki* clearly teaches bonding an upper second substrate 1B to a

lower first substrate 1A, thereby constituting a substrate having a plurality of cavities. However, *Miyawaki* fails to teach or suggest molding as an optional, or alternative, method of forming the hollow packages of *Miyawaki*.

In fact, the purpose of the teachings of *Miyawaki* is to provide a method of packaging a semiconductor device that overcomes the deficiencies of a "mold package" referenced in the Background of the Invention. (*Miyawaki*, col. 1, ll. 15-58.) Although *Miyawaki* generically discloses a "mold package," *Miyawaki* fails to teach or suggest the limitations as presently recited in claim 1.

Specifically, the only reference to molding in *Miyawaki* is the reference to a commonly-used "mold package" or "transfer mold package" mentioned in the background of the invention. (*Id.*) *Miyawaki* is completely devoid of any description of the "mold package" (other than that an epoxy resin comes into close contact with a semiconductor chip) or any teaching relating to any of the steps that are performed to create this "mold package." Thus, even given that *Miyawaki* discloses a "mold package" (whatever that may be), *Miyawaki* clearly fails to teach or suggest the specific steps recited in the present claims, namely, molding sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface in combination with the other limitations recited in claim 1.

With respect to the Examiner's remarks regarding *Miyawaki* not teaching away from the use of conventional mold packages, the Examiner asserts that "Miyawaki does not teach away from a conventional method of molding ... [but instead] ... provides another advantage of sealing the individual packages after they are separated." (*Examiner's Answer*, p. 7, ll. 10-12.) However, the Appellant notes that *Miyawaki* plainly states that the "mold package" referred to by *Miyawaki* is inferior due to parasitic capacitance and deterioration of the characteristics of the semiconductor package and that the teachings of *Miyawaki* have "been conceived to solve [this] problem." (*Miyawaki*, col. 1, ll. 51-58.)

Specifically, as discussed in the Background of the Invention, *Miyawaki* teaches that the "mold package" has parasitic capacitance and deteriorates the characteristics of the semiconductor package. To overcome this problem, a package having a hollow cavity has been used. However, this "hollow package" is inferior in productivity to the

"mold package." Thus, the "present invention" of *Miyawaki* teaches a method of manufacturing a semiconductor device encapsulated in a hollow package (which is clearly different than the "mold package") that prevents deterioration of the high-frequency characteristics of the semiconductor device while ensuring the same productivity and costs as achieved by the mold package." (*See, Id.*, col. 1, ll. 16-58.)

Throughout the entire disclosure, *Miyawaki* repeatedly emphasizes that his embodiments overcome the drawbacks associated with the "mold package" referred to in the Background of the Invention while achieving similar productivity benefits as attained using the "mold package." (*See, at least, Id.*, col. 4, ll. 51-60, and col. 8, ll. 4-7). Thus, *Miyawaki* clearly teaches away from using the referred to "mold package" due to the drawbacks associated with those packages (*e.g.*, parasitic capacitance and deterioration of the characteristics of the semiconductor package).

Moreover, as noted above, even if *Miyawaki* fails to teach away from using the "mold package" referred to in the Background of the Invention, *Miyawaki* still fails to teach or suggest the limitations recited in claim 1 because at no place in *Miyawaki*, either at the location cited by the Examiner or elsewhere, is any specific molding process taught or suggested, let alone one that includes the step of molding sidewalls onto a substrate to form a plurality of cavities, as recited in claim 1.

Accordingly, for the reasons discussed in the Appeal Brief and above, a *prima facie* case of obviousness has not been established because the combination of *Miyawaki* and *Mahulikar* , or *Miyawaki*, *Mahulikar*, and *Song*, fails to yield a method of packaging at least one component including the step of molding sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface, as recited in claim 1, and all claims depending therefrom.

Thus, independent claim 1 and claims 2-7 and 9-11, depending therefrom, are patentable over *Miyawaki* in view of *Mahulikar*, and claim 8 is patentable over *Miyawaki* in view of *Mahulikar* and further in view of *Song*. Accordingly, the Appellant requests that the rejection be withdrawn and the claims allowed.

CONCLUSION

For the reasons advanced above, Appellants respectfully urge that the rejections of claims 1-11 as being unpatentable under 35 U.S.C. §103 are improper. Reversal of the rejections in this appeal is respectfully requested.

Respectfully submitted,

October 13, 2006

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CLAIMS APPENDIX

1. (Original) A method of packaging at least one component, comprising:

providing a lid having a plurality of vent holes;

molding sidewalls onto a substrate to form a plurality of cavities surrounding a component-mounting surface;

mounting a component on the component-mounting surface in each cavity;

applying a curable adhesive to a top surface of the sidewalls;

placing the lid upon the top surface of the sidewalls such that at least one vent hole is aligned with each cavity;

curing said adhesive, said vent hole providing a path for outgassing during curing;

sealing said vent holes to form a component package assembly having a plurality of cavities, separated by sidewalls; and

separating the component package assembly into a plurality of individual component packages.

2. (Original) The method of claim 1, wherein the component comprises electronic circuits.

3. (Original) The method of claim 1 wherein the component is a radio frequency circuit.

4. (Original) The method of claim 1, wherein the top cover and sidewalls are formed of polymers.

5. (Original) The method of claim 1, wherein curing said adhesive comprises heating the adhesive.

6. (Original) The method of claim 1, wherein separating comprises sawing, laser cutting, water cutting, milling, machining, lathing, and combinations thereof.

7. (Original) The method of claim 1 wherein placing the lid upon the sidewalls comprises applying a substantially uniform pressure over each cavity.

8. (Original) The method of claim 1 wherein the applying step comprises screen printing the adhesive on the top surface of the sidewalls.

9. (Original) The method of claim 1 wherein the cavity comprises a low dielectric constant material.

10. (Original) The method of claim 9 wherein the low dielectric constant material is air.

11. (Original) The method of claim 9 wherein the component is a radio frequency circuit.

EVIDENCE APPENDIX

[NONE]

RELATED PROCEEDINGS APPENDIX

[NONE]